C8 17. (Amended) The liquid crystal display system of claim 13, wherein the first image data signal and the second image data signal have a phase difference of 90° or 270°.

Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 1-17 are pending in the application, among which claims 1 and 10 are independent claims. Claims 1-11 and 14-17 are amended to merely correct grammatical errors and for stylish embellishment.

Based on the above amendment and the following Remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and they be withdrawn. Attached hereto is a marked-up version of the changes made to the specifications and claims 1-11 and 14-17 by the current Amendment. The attachment is captioned "Version with Markings to Show Changes Made."

Description of Invention

The invention disclosed in the present Application relates to a liquid crystal display having a dual shift clock wire. The disclosed invention reduces Electro Magnetic Interference (EMI) arising from the transmission of high-speed shift clock signals and data signals.

Rejections Under 35 U.S.C. § 103

On page 2 of the Office Action, the Examiner rejected claims 1-17 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,811,837 issued to Misawa *et al.* ("Misawa") in view of U.S. Patent No. 6,198,307 issued to Garlepp *et al.* ("Garlepp"). However, it is submitted that both independent claims 1 and 10 and their respective dependent claim 2-9 and 11-17 are patentable over the references of record.

Claim 1 recites a liquid crystal display system, comprising a timing controller for sending both the image data signals and a shift clock signal to the data driver. As admitted by the Examiner, the primary reference, Misawa, does not disclose the timing controller. Furthermore, the secondary reference, Garlepp, does not disclose the timing controller as recited in the present Application, either.

The Examiner alleges that Garlepp discloses a timing controller in Fig. 9, item 15 and col. 7, lines 12-37. However, the differential clock driver 15 in Fig. 9 of Garlepp merely generates differential clock signal. Unlike the invention recited in claim 1 of the present Application, the Garlepp device does not send image data signals.

Therefore, Misawa even combined with Garlepp does not disclose nor even suggests the timing controller that is recited in claim 1 of the present Application. Thus, claim 1 is patentable over Misawa and Garlepp.

In addition, unlike the Examiner's allegation, it would not be obvious to combine the Misawa reference with Garlepp reference. As clearly shown in the face of the patent, the Misawa reference is directed to LCD device. However, Garlepp reference is mainly directed to DRAM (Dynamic Random Access Memory) device. One of ordinary skill in the art would not combine these two references without special circumstances. The Examiner failed to suggest any motivations or reasons from the cited references to combine these references. Therefore, one of

ordinary skill in the art would not combine the LCD device with the technology for DRAM and it is not obvious to adopt the timing controller of Garlepp in the LCD device of Misawa.

Thus, claim 1 is patentable over Misawa and Garlepp. Likewise, claims 2-9 that are dependent from claim 1 are also patentable over the references of record.

Likewise, claim 10 is also patentable over Misawa and Garlepp. Claim 10 recites a liquid crystal display system, comprising a circuit board including a timing controller for generating a first image data signal and a second image data signal and generating a first shift clock signal and a second shift clock signal ...

As discussed previously, Misawa even combined with Garlepp neither discloses nor suggests such a timing controller as recited in claim 10 of the present Application. Therefore, claim 10 is patentable over Misawa and Garlepp. Likewise, claims 11-17 that are dependent from claim 10 are also patentable over the references of record.

Throughout pages 4-6, the Examiner alleges that claims 2-9 and 11-17 are not patentable for various reasons, referring to the references of record. However, as discussed previously, claims 2-9 and 11-17 are respectively patentable over claims 1 and 10 that are patentable over Misawa and Garlepp. Therefore, dependent claims 2-9 and 11-17 are also patentable over such references.

As such, it is respectfully requested that all the rejections and objections over claims 1-17 be withdrawn and pass those claims to issuance.

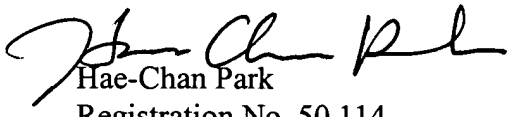
Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner

reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete response has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment is respectfully requested.

Respectfully submitted,



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Version with Markings to Show Changes Made

Amendments

In the Specifications:

Please enter the following amendments.

Page 1, line 15, change "agate line" into – a gate line –.

Page 3, line 17, change "shift dock signal" into – shift clock signal –.

Page 3, line 18, after "invention", insert – , –.

Page 7, line 5, change "a R, G, B color filter layer" into – an R, G, B color filter layer –.

Page 11, line 21, after "opposite", change "phrase" into – phase –.

In the Claims:

Please amend claims 1-11 and 14-17 as follows.

1. (Twice Amended) A liquid crystal display system, comprising:

a liquid crystal display panel including a plurality of data lines, a plurality of gate lines intersecting the data lines, and a plurality of pixel electrodes arranged in a matrix type and each having a switch connected to one of the gate lines and one of the data lines;

a gate driver for successively applying a gate voltage to the gate lines to turn on the switches;

a data driver for applying a gray voltage, corresponding to image data signals, to the data lines;

a timing controller for sending both the image data signals and a shift clock signal to the data driver,

a first signal wire through which the shift clock signal is transmitted to said data driver; and

a second signal wire through which a first clock signal having a frequency equal to the shift clock signal but having a phase difference of 90° to 270° is transmitted to a ground.

2. (Twice Amended) The liquid crystal display system of claim 1, wherein the second signal wire is connected to the ground through a predetermined resistance value.

3. (Amended) The liquid crystal display system of claim 2, wherein the first clock signal is generated in the timing controller.

4. (Amended) The liquid crystal display system of claim 2, wherein the first signal wire and the second signal wire are provided on a circuit board.

5. (Amended) The liquid crystal display system of claim 4, wherein the circuit board is a multi-layered printed circuit board and the first signal wire and the second signal wire are formed in parallel on the same layer.

6. (Amended) The liquid crystal display system of claim 4, wherein the circuit board is a multi-layered printed circuit board and the first signal wire and the second signal wire are formed on different layers.

7. (Amended) The liquid crystal display system of claim 1, wherein the first clock signal

has a 180° phase difference from the shift clock signal.

8. (Amended) The liquid crystal display system of claim 7, wherein the data driver comprises a plurality of data driver integrated circuits for receiving the image data signals and the shift clock signal from the timing controller and applying the gray voltage corresponding to the image data signals to the data lines of the LCD panel.

9. (Amended) The liquid crystal display system of claim 8, wherein the data driver integrated circuits comprise:

a shift register for shifting and storing the image data signals in synchronization with the shift clock signal after receiving the image data signals from the timing controller;

a D/A converter receiving the image data signals stored in the shift register and converting the image data signals to a corresponding gray voltage; and

an output buffer for temporarily storing the gray voltage output from the D/A converter, and applying the gray voltage to the data lines of the liquid crystal display panel line by line [in units of lines].

10. (Amended) A liquid crystal display system, comprising:

a liquid crystal display panel including a plurality of data lines, a plurality of gate lines intersecting the data lines, and a plurality of pixel electrodes arranged in a matrix type and each having a switch connected to one of the gate lines and one of the data lines;

a gate driver for successively applying a gate voltage to the gate lines to turn on the switches;

a circuit board including:

a timing controller for generating a first image data signal and a second image data signal and generating a first shift clock signal and a second shift clock signal with a phase difference of 90° to 270° that respectively shift the first image data signal and the second image data signal;[,]

a first image data signal wire and a second image data signal wire through which the first image data signal and the second image data signal are respectively transmitted;[,] and

a first shift clock signal wire and a second shift clock signal wire through which the first shift clock signal and the second shift clock signal are respectively transmitted;

a data driver receiving the first image data signal and the second image data signal and the first shift clock signal and the second shift clock signal from the timing controller, and applying a gray voltage corresponding to the first image data signal and the second image data signal to the data lines.

11. (Amended) The liquid crystal display system of claim 10, wherein the first image data signals are odd image data signals, and the second image data signals are even image data signals.

14. (Amended) The liquid crystal display system of claim 13, wherein the first image data signal and the second image data signal have a phase difference of 180°.

15. (Amended) The liquid crystal display system of claim 14, wherein the first image data

signal is synchronized to a rising edge of the first shift clock signal, and the second image data signals is synchronized to a falling edge of the second shift clock signal.

16. (Amended) The liquid crystal display system of claim 14, wherein a pulse width of the first shift clock signal and the second shift clock signal falls within the interval of a high signal or a low signal of the odd image data signal and the even image data signal[s].

17. (Amended) The liquid crystal display system of claim 13, wherein the first image data signal and the second image data signal[s] have a phase difference of 90° or 270°.